What is claimed is:

1. A Flash memory system comprising:

at least one Flash memory device, wherein the at least one Flash memory device contains a memory array with a plurality of floating gate memory cells arranged in a plurality of erase blocks, and wherein each erase block of the plurality of erase blocks contains a plurality of sectors, and each sector contains a user data area and an overhead data area;

wherein the erase blocks of the at least one Flash memory device are arranged in pairs into a plurality of super blocks; and

a control circuit adapted to control data accesses to the sectors of the erase block pair of a selected super block such that user data access and overhead data accesses are directed to differing erase blocks of the super block.

2. The Flash memory system of claim 1, wherein the data access is one of a write access and a read access.

3. The Flash memory system of claim 1, wherein at least one super block of the plurality of super blocks contains erase blocks from a first Flash memory device and a second Flash memory device.

4. The Flash memory system of claim 1, wherein each super block of the plurality of super blocks contain two or more erase blocks.

5. The Flash memory system of claim 1, wherein the Flash memory system is one of a PCMCIA-ATA compatible system, a Compact Flash (CF) card, a USB Flash card, and a multimedia card (MMC).

6. The Flash memory system of claim 1, wherein each erase block of the plurality

of erase blocks contains at least 16 sectors, and each sector contains a user data area of at least 512 bytes and an overhead data area.

7. The Flash memory system of claim 1, wherein each sector is adapted to contain multiple logical sectors.

8. The Flash memory system of claim 1, wherein the control circuit includes a dedicated data splitting circuit that is adapted to split data accesses to the sectors of the erase block pair of a super block of the plurality of super blocks such that the user data access and overhead data access are directed to differing erase blocks of the super block.

9. The Flash memory system of claim 1, wherein the plurality of sectors of each erase block are sequentially addressed and wherein the control circuit is adapted to access the overhead data area of a sector m of one erase block of the super block when a user data area of a selected sector m of the other erase block of the super block is accessed.

10. The Flash memory system of claim 1, wherein the plurality of sectors of each erase block are sequentially addressed 0 to x, where x is the address of the highest addressed sector of each erase block and wherein the control circuit is adapted to access the overhead data area of a sector x-m of one erase block of the super block when a user data area of a selected sector m of the other erase block of the super block is accessed.

11. The Flash memory system of claim 1, wherein the plurality of sectors of each erase block in the super block are sequentially addressed, with one erase block holding even addressed sectors and the other erase block holding odd addressed sectors, and wherein the control circuit is adapted to access the overhead data area of a sector m+1 when a user data area of a selected sector m is accessed.

12. The Flash memory system of claim 11, wherein the user data area of the selected sector m is accessed simultaneously with an overhead data area of a sector m-1.

13. The Flash memory system of claim 1, wherein the plurality of erase blocks are sequentially addressed and wherein the erase block pair of each super block are addressed Erase Block N and Erase Block N+Y, where N is a base address and Y is an offset.

14. The Flash memory system of claim 1, wherein the plurality of erase blocks are sequentially addressed and wherein the erase block pair of each super block are addressed Erase Block N and Erase Block Y-N, where N is a base address and Y is the address of the highest addressed erase block of the plurality of erase blocks.

15. The Flash memory system of claim 1, wherein the plurality of erase blocks are sequentially addressed and wherein the erase block pair of each super block are addressed Erase Block N and Erase Block N +1.

16. A non-volatile memory device comprising:

a memory array containing a plurality of floating gate memory cells arranged into a plurality of sectors in a plurality of erase blocks, each sector containing a user data area and an overhead area;

wherein the plurality of erase blocks are arranged in pairs into a plurality of super blocks; and

wherein non-volatile memory device is adapted to execute a data access such that a user data area of a selected first sector of a first erase block of a super block pair also accesses an overhead data area of an associated first sector of a second erase block of the erase block pair of the super block.

17. The non-volatile memory device of claim 16, wherein the data accesses are one of a write access and a read access.

18. The non-volatile memory device of claim 16, wherein a data splitting circuit is adapted to access the user data area of the selected first sector of the first erase block of the super block pair and to access the overhead data area of the associated first sector of the second erase block of the erase block pair.

19. The non-volatile memory device of claim 16, wherein a following data access to the super block accessing the next sequential sector address accesses the user data area of the first sector of the second erase block of the super block pair and accesses the overhead data area of the first sector of the first erase block of the erase block pair of the super block.

20. The non-volatile memory device of claim 16, wherein a following data access to the super block accessing the next sequential sector address accesses the user data area of a second sector of the second erase block of the super block pair and accesses the overhead data area of a second sector of the first erase block of the erase block pair of the super block.

21. The non-volatile memory device of claim 16, wherein a following data access to the super block accessing the next sequential sector address accesses the user data area of a second sector of the first erase block of the super block pair and accesses the overhead data area of a second sector of the second erase block of the erase block pair of the super block.

22. A Flash memory system comprising:

one or more Flash memory devices, each Flash memory device having a memory array containing a plurality of floating gate memory cells arranged into a plurality of sectors in a plurality of erase blocks;

wherein the plurality of erase blocks of the one or more Flash memory devices are associated into pairs of erase blocks; and

wherein the Flash memory system is adapted to access user data from a selected sector of an erase block of a pair of associated erase blocks and access the associated overhead data from an overhead data area of a sector of the associated erase block of the erase block pair.

23. The Flash memory system of claim 22, wherein a data splitting circuit is adapted to access a user data area of the selected sector of the erase block of the pair of associated erase blocks and to access the associated overhead data from an overhead data area of the sector of the associated erase block of the erase block pair.

24. The Flash memory system of claim 22, wherein at least one pair of erase blocks contains erase blocks from a first Flash memory device and a second Flash memory device.

25. The Flash memory system of claim 22, wherein a control circuit is adapted to erase both erase blocks of an erase block pair concurrently.

26. The Flash memory system of claim 22, wherein a control circuit is adapted to allocate both erase blocks of an erase block pair for utilization at the same time.

27. The Flash memory system of claim 22, wherein a control circuit is adapted to replace both erase blocks of the erase block pair with a replacement erase block pair when an erase block of the erase block pair becomes damaged.

28. The Flash memory system of claim 22, wherein a control circuit is adapted to replace a single erase block of the erase block pair with a replacement erase block when the erase block of the erase block pair becomes damaged.

29. The Flash memory system of claim 22, wherein a control circuit is adapted to map a logical address to a physical address of the plurality of erase blocks.

30. A Flash memory device comprising:

a memory array with a plurality of floating gate memory cells arranged in a plurality of erase blocks, wherein the erase blocks are arranged in pairs into a plurality of super blocks, and wherein each erase block of the plurality of erase blocks contains a plurality of sectors, and each sector contains a user data area and an overhead data area; and

a control circuit adapted to perform data accesses to the sectors of the erase block pair of a super block such that user data access and overhead data accesses are directed to differing erase blocks of the super block.

31. The Flash memory device of claim 30, wherein each sector is adapted to contain multiple logical sectors in the user data area and overhead data area.

32. The Flash memory device of claim 30, wherein the control circuit includes a dedicated data splitting circuit that is adapted to split data accesses to the sectors of the erase block pair of a super block of the plurality of super blocks such that the user data access and overhead data access are directed to differing erase blocks of the super block.

33. The Flash memory device of claim 30, wherein the plurality of sectors of each erase block are sequentially addressed and wherein the control circuit is adapted to access the overhead data area of a sector m of one erase block of the super block when a user data area of a selected sector m of the other erase block of the super block is accessed.

34. The Flash memory device of claim 30, wherein the plurality of sectors of each

erase block are sequentially addressed 0 to x, where x is the address of the highest addressed sector of each erase block and wherein the control circuit is adapted to access the overhead data area of a sector x-m of one erase block of the super block when a user data area of a selected sector m of the other erase block of the super block is accessed.

35. The Flash memory device of claim 30, wherein the plurality of sectors of each erase block in the super block are sequentially addressed, with one erase block holding even addressed sectors and the other erase block holding odd addressed sectors, and wherein the control circuit is adapted to access the overhead data area of a sector m+1 when a user data area of a selected sector m is accessed.

36. The Flash memory device of claim 35, wherein the user data area of the selected sector m is accessed simultaneously with an overhead data area of a sector m-1.

37. A Flash memory device comprising:

a memory array containing a plurality of floating gate memory cells arranged into a plurality of sectors in a plurality of erase blocks, wherein the plurality of erase blocks are associated into pairs of erase blocks; and

wherein the Flash memory device is adapted to access user data from a selected sector of an erase block of a pair of associated erase blocks and access the associated overhead data from an overhead data area of a sector of the associated erase block of the erase block pair.

38. The Flash memory device of claim 37, wherein a data splitting circuit is adapted to access a user data area of the selected sector of the erase block of the pair of associated erase blocks and to access the associated overhead data from an overhead data area of the sector of the associated erase block of the erase block pair.

39. The Flash memory device of claim 37, wherein a control state machine circuit is adapted to erase both erase blocks of an erase block pair concurrently.

40. The Flash memory device of claim 37, wherein a control state machine circuit is adapted to allocate both erase blocks of an erase block pair for utilization at the same time.

41. The Flash memory device of claim 37, wherein a control state machine circuit is adapted to replace both erase blocks of the erase block pair with a replacement erase block pair when an erase block of the erase block pair becomes damaged.

42. A super block memory structure comprising:

a pair of erase blocks having a plurality of floating gate memory cells arranged in plurality of sectors, each sector having a user data area and an overhead data area; and

wherein a data access to a user data area of a selected sector of an erase block of the erase block pair accesses an associated overhead data from an overhead data area of a sector of the other erase block of the erase block pair.

43. The super block memory structure of claim 42, wherein the overhead data contains at least one error correction code (ECC).

44. A data splitting circuit comprising:

a data circuit adapted to receive a data access request and concurrently access a user data area of a sector of a first erase block and an overhead data area of a sector of a second erase block.

45. The data splitting circuit of claim 44, wherein the data circuit is adapted to write data to the user data area of the sector of the first erase block and write data to the overhead data area of the sector of the second erase block for each write

access of the first erase block.

46. The data splitting circuit of claim 44, wherein the data circuit is adapted to read data from the user data area of the sector of the first erase block and read data from the overhead data area of the sector of the second erase block for each read access of the first erase block.

47. The data splitting circuit of claim 44, wherein the user data area of a selected sector m is accessed simultaneously with an overhead data area of a sector m-1.

48. A data splitting circuit comprising:
a data circuit adapted to receive a data access request and access a user data area of a first sector and access an overhead data area of a second sector.

49. The data splitting circuit of claim 48, wherein the data circuit is adapted to access the first sector from a first erase block and access the second sector from a second erase block.

50. The data splitting circuit of claim 48, wherein the user data area of a selected sector m is accessed simultaneously with an overhead data area of a sector m-1.

51. A method of operating a Flash memory system comprising:
receiving a memory access request;
accessing a user data area of a sector of an erase block of a plurality of erase blocks of one or more Flash memory devices; and
concurrently accessing an overhead data area of a sector of an associated erase block of the plurality of erase blocks.

52. The method of claim 51, wherein the erase block is from a first Flash memory device and the associated erase block is from a second Flash memory device.

53. The method of claim 51, wherein the sectors of the erase block and the associated erase block are sequentially addressed, with one erase block holding even addressed sectors and the other erase block holding odd addressed sectors.

54. The method of claim 53, wherein accessing a user data area of a sector of an erase block and concurrently accessing an overhead data area of a sector of an associated erase block further comprises concurrently accessing the overhead data area of a sector m+1 when a user data area of a selected sector m is accessed.

55. The method of claim 54, wherein the user data area of the selected sector m is accessed simultaneously with an overhead data area of a sector m-1.

56. The method of claim 51, wherein accessing a user data area of a sector of an erase block and accessing an overhead data area of a sector of an associated erase block further comprises accessing the same relative sector address in each erase block.

57. The method of claim 51, wherein accessing a user data area of a sector of an erase block and accessing an overhead data area of a sector of an associated erase block further comprises accessing a user data area of a sector of an erase block and accessing an overhead data area of a sector of an associated erase block wherein the plurality of erase blocks are sequentially addressed and wherein the erase block and the associated erase block are addressed Erase Block N and Erase Block N+Y, respectively, where N is a base address and Y is an offset.

58. A method of operating a Flash memory device comprising:
receiving a memory access request;

accessing a user data area of a sector of an erase block of a plurality of erase blocks of a Flash memory array; and

accessing an overhead data area of a sector of an associated erase block of the plurality of erase blocks in response to accessing the user data area of the erase block.

59. The method of claim 58, wherein the erase block and the associated erase block are associated in a super block pair.

60. The method of claim 58, wherein the sectors of the erase block and the associated erase block are sequentially addressed, with one erase block holding even addressed sectors and the other erase block holding odd addressed sectors.

61. The method of claim 60, wherein accessing a user data area of a sector of an erase block and accessing an overhead data area of a sector of an associated erase block further comprises accessing the overhead data area of a sector m+1 when a user data area of a selected sector m is accessed.

62. The method of claim 58, wherein accessing a user data area of a sector of an erase block and accessing an overhead data area of a sector of an associated erase block further comprises accessing a user data area of a sector of an erase block and accessing an overhead data area of a sector of an associated erase block wherein the plurality of erase blocks are sequentially addressed and wherein the erase block and the associated erase block are addressed Erase Block N and Erase Block N +1, respectively.

63. A method of data splitting in a memory system comprising:

dividing a data access request into a user data access request and an overhead data access request;

accessing a sector of a first erase block in response to the user data access

request; and

accessing a sector of a second erase block in response to the overhead data access request.

64. The method of claim 63, wherein accessing a sector of a second erase block in response to the overhead data access request further comprises simultaneously accessing a sector of a second erase block in response to the overhead data access request and a second user data access request from a second data access request.

65. The method of claim 63, wherein accessing a sector of a first erase block in response to the user data access request further comprises simultaneously accessing a sector of a first erase block in response to the user data access request and an overhead data request from a third data access request.

66. A computer system comprising:

a host coupled to a Flash memory device, wherein the Flash memory device comprises:

a memory array containing a plurality of floating gate memory cells arranged into a plurality of sectors in a plurality of erase blocks, each sector containing a user data area and an overhead area;

wherein the plurality of erase blocks are arranged in pairs into a plurality of super blocks; and

wherein a data access to a user data area of a selected sector of an erase block of a super block also accesses an overhead data area of an associated sector of the other erase block of the erase block pair of the super block.

67. The computer system of claim 66, wherein the Flash memory device is adapted to appear to the host as a rewriteable storage device.

68. The computer system of claim 66, wherein the host is one of a processor and an external memory controller.

69. The computer system of claim 66, wherein an interface to the Flash memory device is compatible with a mass storage device.

70. The computer system of claim 66, wherein an interface to the Flash memory device is one of a PCMCIA-ATA, a Compact Flash (CF), a USB Flash, and a multimedia card (MMC) compatible interface.

71. A method of data splitting in a memory system comprising:
receiving a sequence of data accesses to a memory system;
dividing the sequence of data accesses into user data accesses and overhead data accesses; and
sequentially accessing the memory system such that an access to a sector of an erase block concurrently accesses a selected user data and an overhead data for a previous user data access.

72. The method of claim 71, wherein sequentially accessing the memory system such that an access to a sector of an erase block concurrently accesses a selected user data and an overhead data for a previous user data access further comprises accessing a selected user data m and an overhead data for user data access m-1.

73. The method of claim 72, wherein a final data access in the sequence of data accesses, accesses the user data in a selected sector m and the overhead data in a sector m+1.

74. The method of claim 73, wherein a final data access in the sequence of data accesses, accesses the user data in a final sector and the overhead data in a first

sector.

75. The method of claim 71, wherein sequentially accessing the memory system such that an access to a sector of an erase block concurrently accesses a selected user data and an overhead data for a previous user data access further comprises sequentially accessing the memory system such that accesses to sequential sectors alternate between a first and a second erase block.

76. The method of claim 71, wherein sequentially accessing the memory system such that an access to a sector of an erase block concurrently accesses a selected user data and an overhead data for a previous user data access further comprises simultaneously accessing the overhead data for the previous user data access with the current access to the selected user data.

77. An erase block physical sector comprising:
a user data area; and
an overhead data area, wherein the overhead data stored in the overhead data area of the erase block sector is associated with the user data of a different erase block physical sector.

78. The erase block physical sector of claim 77, wherein the erase block physical sector is adapted to contain multiple logical sectors.

79. The erase block physical sector of claim 78, wherein the erase block physical sector contain at least four sequentially addressed logical sectors of 512-bytes each.

80. The erase block physical sector of claim 77, wherein the overhead data area is adapted to contain multiple logical overhead areas, wherein each logical overhead area corresponds to a logical sector of the different erase block

physical sector.

81. The erase block physical sector of claim 77, wherein the overhead data area is adapted to contain at least one error correction code (ECC).

82. The erase block physical sector of claim 77, wherein the user data area and the overhead data area have relative addresses within the erase block physical sector and wherein the user data area has a relative address that is higher than the overhead data area.

83. An address control circuit comprising:
a control circuit coupled to a host interface;
a first and second address registers coupled to the control circuit;
an address multiplexer coupled to the first and second address registers and to a Flash memory interface; and
wherein the address control circuit is adapted to load a data access request containing a data address from the host interface and address sequentially addressed Flash memory physical sectors of a selected superblock as data is accessed by a host, where the superblock contains a first and second erase blocks.

84. The address control circuit of claim 83, wherein the address control circuit is adapted to sequentially access physical sectors of the first and second erase blocks in a pattern that alternates between physical sectors of the first and second erase block as the physical sectors of the superblock are sequentially accessed.

85. The address control circuit of claim 83, wherein the data access loaded from the host contains an initial address offset in an initially accessed physical sector of the superblock.

86. The address control circuit of claim 83, wherein each address register has at least a first portion and second portion.

87. The address control circuit of claim 86, wherein the first portion is adapted to contain a row address and second portion is adapted to contain a column address.

88. The address control circuit of claim 86, wherein the address control circuit is adapted to reset the second portion of the first and second address registers to zero when a physical sector boundary is crossed.

89. The address control circuit of claim 86, wherein the address control circuit is adapted to reset the first portion of the first and second address registers to zero to after a final physical sector of the superblock is accessed.

90. The address control circuit of claim 86, wherein the address control circuit is adapted to increment the first portion of the first and second address registers after a physical sector boundary of the second erase block is crossed.

91. The address control circuit of claim 86, wherein the address control circuit is adapted to switch the currently selected address register of the first and second address registers that is coupled to the Flash memory interface after a physical sector boundary of the first or second erase block is crossed.

92. A split data error correction code (ECC) circuit comprising:
a control circuit coupled to an error correction code (ECC) circuit; and
wherein the split data ECC circuit is adapted to generate at least one ECC code from user data of a first physical sector during a data access, and where the split data ECC circuit is adapted to write the at least one ECC code to a

second physical sector if the data access is a write access or compare the at least one generated ECC code with at least one ECC code stored in a second physical sector if the data access is a read access.

93. The split data error correction code (ECC) circuit of claim 92, wherein first and second physical sectors contain multiple logical sectors and ECC code data areas, and wherein the split data ECC circuit is adapted to generate an ECC code for each accessed logical sector of the first physical sector.

94. The split data error correction code (ECC) circuit of claim 92, wherein the data access is a sequential access that progresses from the first physical sector to the second physical sector.

95. The split data error correction code (ECC) circuit of claim 92, wherein the split data ECC circuit further comprises:

a RAM storage circuit coupled to the control circuit and the ECC circuit, wherein the split data ECC circuit is adapted to store the at least one generated ECC code in the RAM storage unit.

96. The split data error correction code (ECC) circuit of claim 92, wherein the first and second physical sectors are from differing erase blocks of a superblock.

97. The split data error correction code (ECC) circuit of claim 92, wherein the ECC circuit is adapted to generate and compare ECC data codes to detect data errors during a data read access.

98. The split data error correction code (ECC) circuit of claim 97, wherein the ECC circuit is adapted to correct user data during a data read access.

99. A NAND Flash memory system comprising:

at least one NAND Flash memory device, wherein the at least one Flash memory device contains a NAND architecture memory array with a plurality of floating gate memory cells arranged in a plurality of erase blocks, and wherein each erase block of the plurality of erase blocks contains a plurality of physical sectors, and each physical sector contains a user data area and an overhead data area;

wherein the erase blocks of the at least one NAND Flash memory device are arranged in pairs into a plurality of super blocks;

a control circuit adapted to control data accesses to the physical sectors of the erase block pair of a selected super block; and

wherein the plurality of physical sectors of each erase block in the super block are sequentially addressed, with one erase block holding even addressed physical sectors and the other erase block holding odd addressed physical sectors, and wherein the control circuit is adapted to access the overhead data area of a physical sector m+1 when a user data area of a selected physical sector m is accessed.